REMARKS

In section 1 of the Office Action, the Examiner objects to the specification as missing headings. Headings have been added to the specification accordingly (see page 2). It is believed that this objection has been overcome.

In section 3 of the Office Action, claims 1-4 and 7-17 are rejected under 35 USC 102(b) as being anticipated by Harari et al. (US Patent No. 5,504,760). In section 4, claims 5-6 and 18-20 are rejected under 35 USC 103(a) as being unpatentable over Harari et al. in view of Perner et al. (US Patent No. 6,456,525). These rejections are respectfully traversed.

Harari et al. and Perner et al., standing alone or in combination, fail to disclose, teach, or suggest, *inter alia*, the following limitations recited by claim 1 of the present application:

"forming erasure information for the block of stored ECC encoded data, using the obtained parametric values" and

"error correction decoding the block of stored ECC encoded data with reference to the erasure information".

Harari et al. is related to techniques for optimum erasing and programming of EEPROMs. In particular, Harari et al. discloses a method for determining which data encoding scheme has been used for programming the retrieved data by examining whether an error correction code of the data indicates an error. Harari et al. nowhere teaches the generation of erasure

data using parametric testing or the subsequent use of the erasure data in error correction decoding, as recited by claim 1 of the present application.

First, Harari belongs to a different storage technology, namely EEPROM devices and to the resolution of a particular problem they have, i.e., that repeated program erase cycles in such devices inevitably causes them to fail. Harari describes a variety of controlled erasure techniques that are used to prolong the life of EEPROM devices.

Harari discusses only briefly the question of defective cells and then only discusses two types of defective cells, namely the "stuck 0" cells and "stuck 1" cells. The passage between col. 20 line 51 and col. 22 line 40 of Harari that the Examiner refers to does not relate to the management of even these types of defective cells (this is discussed elsewhere) but rather relates to a scheme to render statistically uniform the program-erase cycling histories of sectors in an EEPROM array. Two encoding schemes are either randomly or alternately applied to a sector to scramble the user data pattern. In one of several arrangements described, EEC codes are used to distinguish between the encoding schemes that were applied to each sector, by detecting ECC errors.

Thus, the question of handling bits for which no logical value can be obtained or where the logical value is considered unreliable is not addressed at all by Harari. In the description of the present application, bits of this type are identified using parametric data (i.e. physically measured values) are used to identify such bits and to generate so-called "erasure data" that

is then used to increase the precision of an ECC applied to the data that can be read. The information referred to as "erasure data" in the present application has nothing to do with the program-erase cycles of an EEPROM, but this may be what is confusing the Examiner.

Perner et al. discloses a data storage device including a resistive cell cross point memory array. Each memory cell has a memory element and a resistive element connected in series with the memory element. The resistive elements then attenuate the sneak path currents flowing through shorted memory elements during read operation. Such data storage device is a Magnetic Random Access Memory (MRAM) device.

Perner et al. is cited with respect to features of claims 5-6 and 18-20, in that an MRAM device is disclosed. The Examiner does not show that Perner et al. teaches or suggests the above-quoted features of claim 1. Indeed, Perner et al. does not disclose any feature similar to those features, because it seems that Perner et al. does not concern forming erasure information by parametric values.

MPEP 2131 states that a "claim is anticipated only if **each and every element** as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," quoting *Verdegaal Bros v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987). Under MPEP 2143, to establish a prima facie case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Since the cited references do not disclose the above-quoted limitations of claim 1, the Applicants respectfully submit that claim 1 is patentable.

Claims 2-16 and 18 are also patentable, at least by virtue of their dependency form claim 1.

Similarly, claim 17 and claim 19 recite, in part, "an array controller for obtaining parametric values from a set of the storage cells and generating a block of stored ECC encoded data using the obtained parametric values, including forming erasure information for the block of stored ECC encoded data using the obtained parametric values" and "an ECC decoding unit for decoding the block of stored ECC encoded data with reference to the erasure information". Claims 17 and 19 are patentable for the same reasons as claim 1. Claim 20 is patentable, at least by virtue of its dependency from claim 19.

The Applicants have attempted to address all of the issues raised by the Examiner in the Office Action as the Applicants understand them. It is believed that the application is now in condition for allowance. If any point requires further explanation, the Examiner is invited to telephone Troy Cai at (323) 934-2300 or e-mail Troy Cai at tcai@ladasparry.com.

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account No. 12-0415. In particular, if this response is not timely filed, then the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136 (a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

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